UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,497	10/27/2000	Ahmadreza Rofougaran	40882/CAG/B600	3845

23363 7590 07/08/2003

CHRISTIE, PARKER & HALE, LLP
350 WEST COLORADO BOULEVARD
SUITE 500
PASADENA, CA 91105

EXAMINER
MILORD, MARCEAU

ART UNIT	PAPER NUMBER
2682	16

DATE MAILED: 07/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/698,497	Applicant(s) ROFOUGARAN ET AL.	
	Examiner Marceau Milord	Art Unit 2682	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hilbert (US Patent No 5983082) in view of Miyazaki (US Patent No 5642001) and Siwiak et al (US Patent No 5276912).

Regarding claim 1, Hilbert discloses a circuit (fig. 8), comprising: a logic circuit (420 of fig. 8) having a power input and a power return; a capacitor (805 or 806 of fig. 8; col. 11, line 21- col. 12, line 13); a first resistor (814 of fig. 8) having a first end coupled to the power input and a second end to couple to a power source (col. 12, lines 26 -32); and a second resistor (815 of fig. 8) having a first end coupled to the power return and a second end to couple to a power source return (col. 12, line 33- col. 13, line 65 ; col. 14, lines 11- 65).

However, Hilbert does not specifically disclose a capacitor coupled across the power input and the power return. ; and a first resistor having a first end coupled to the power input and a second end to couple to a power source.

On the other hand, Miyazaki, from the same field of endeavor, discloses a logic circuit having a first current source which supplies an overdrive current and a second current source which supplies an ordinary current smaller than overdrive current (figs. 1-2; col. 3, lines 7-21; col. 5, lines 1- 30; col. 6, lines 31-67).

Siwiak et al discloses in figure 4, an RF power amplifier 120 where a power supply voltage Vs is applied to the drain of FET 122, through an RF choke 123, and a capacitor 126 is disposed between the drain of the FET 122 and an impedance transformation network 129 (figs. 4-6; col. 3, line 1- col. 4, line 55; col. 5, lines 8-65). It is considered that the capacitors 126 and 206 in figures 4 and 6 are coupled across the power input and the power return. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Siwiak to the modified system of Miyazaki and Hilbert in order to minimize power consumption.

Regarding claims 2- 5, Hilbert as modified discloses a circuit (fig. 8), comprising: a logic circuit (420 of fig. 8) wherein the logic circuit comprises a differential circuit; wherein the two logic gates each comprises an inverter (col. 11, lines 21-66).

Regarding claims 7 and 16, Hilbert as modified discloses a circuit (fig. 8), comprising: a logic circuit (420 of fig. 8) wherein the CMOS inverters each comprises a p-channel transistor having a source coupled to the power input, a gate, and a drain, and an n-channel transistor having a source coupled to the power return, a gate coupled to the gate of the p-channel transistor to form an input node, and a drain coupled to the drain of the p-channel transistor to form output node (col. 11, line 21- cot. 12, line 32), the differential circuit further having a differential input comprising the input nodes for each of the CMOS inverters, and a differential output comprising the output nodes for each of the CMOS inverters (cot. 13, line Scot. 14, line 60).

Regarding claim 8, Hilbert discloses a circuit (fig. 8), comprising: logic means (809 of fig. 8) for performing a logic function (col. 11, line 21- col. 12, line 13); charge means (805 or

806 of fig. 8) for storing a charge across the logic means; and isolation means (814 of fig. 8; col. 12, line 33- col. 13, line 65; col. 14, lines 11- 65).

However, Hilbert does not specifically disclose an isolation means for isolating the charge means from a power source.

On the other hand, Miyazaki, from the same field of endeavor, discloses a logic circuit having a first current source which supplies an overdrive current and a second current source which supplies an ordinary current smaller than overdrive current (figs. 1-2; col. 3, lines 7-21; col. 5, lines 1- 30; col. 6, lines 31-67).

Siwiak et al discloses in figure 4, an RF power amplifier 120 where a power supply voltage Vs is applied to the drain of FET 122, through an RF choke 123, and a capacitor 126 is disposed between the drain of the FET 122 and an impedance transformation network 129 (figs. 4-6; col. 3, line 1- col. 4, line 55; col. 5, lines 8-65). It is considered that the capacitors 126 and 206 in figures 4 and 6 are coupled across the power input and the power return. Since the capacitors 126 and 206 can be applied across this logic circuit, they are considered as isolation means for isolating the charge means from a power source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Siwiak to the modified system of Miyazaki and Hilbert in order to minimize power consumption.

Regarding claims 9-10, Hilbert as modified discloses a circuit (fig. 8), comprising: a logic circuit (420 of fig. 8) wherein the charge means comprises a capacitor (805 or 806 of fig. 8); and the isolation means comprises a first resistor (814 of fig. 8) to couple a first end of the capacitor to the power source (col. 12, lines 26 32), a second resistor (815 of fig. 8) to

couple a second end of the capacitor to a return line for the power source (col. 12, line 33- col. 13, line 65; col. 14, lines 11- 65).

Claims 11-15 contain similar limitations addressed in claims 2-7, and therefore are rejected under a similar rationale.

Regarding claims 17-18, Hilbert discloses a method (fig. 3 and fig. 8) of suppressing noise during the switching of a differential circuit having differential inputs and outputs, comprising: charging a capacitor (805 or 806 of fig. 8) through a resistor (814 of fig. 8; col. 11, line 21- col. 12, line 13); applying a signal transition at the differential inputs (col. 9, line 22col. 10, line 66); and circulating charge between the differential outputs (col. 12, lines 26 -32); compensating for loss of the charge on the capacitor during the circulation of charge (col. 12, line 33- col. 13, line 65 ; col. 14, lines 11- 65).

However, Hilbert does not specifically disclose the features of circulating charge between the differential outputs through the capacitor; compensating for loss of the charge on the capacitor during the circulation of charge by recharging the capacitor through the resistor.

On the other hand, Miyazaki, from the same field of endeavor, discloses a logic circuit having a first current source which supplies an overdrive current and a second current source which supplies an ordinary current smaller than overdrive current (figs. 1-2; col. 3, lines 7-21; col. 5, lines 1- 30; col. 6, lines 31-67).

Siwiak et al discloses in figure 4, an RF power amplifier 120 where a power supply voltage Vs is applied to the drain of FET 122, through an RF choke 123, and a capacitor 126 is disposed between the drain of the FET 122 and an impedance transformation network 129 (figs. 4-6; col. 3, line 1- col. 4, line 55; col. 5, lines 8-65). It is considered that the capacitors 126 and

206 in figures 4 and 6 are coupled across the power input and the power return. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Siwiak to the modified system of Miyazaki and Hilbert in order to minimize power consumption.

Regarding claim 19, Hilbert as modified discloses a method (fig. 8) of suppressing noise during the switching of a differential circuit having differential inputs and outputs (col. 9, line 22- col. 10, line 66), comprising clocking the differential circuit after a transition of the signal at the differential output, the circulation of the charge being initiated by clocking the differential circuit, the resistor and capacitor having a time constant that is less than half the clocking frequency (col. 7, line 28- col. 8, line 67).

Regarding claims 20-22, Hilbert discloses an integrated circuit (fig. 4 and fig. 8), comprising: a differential circuit having a power input (col. 6, lines 10-65); the differential circuit further comprises a power return (col. 7, line 28- col. 8, line 67; col. 11, line 21- col. 12, line 13).

However, Hilbert does not specifically disclose an inductor having a first end coupled to the power input and a second end to couple to a power source; and a second inductor having a first end coupled to the power return and a second end to couple to a power source return.

On the other hand, Miyazaki, from the same field of endeavor, discloses a logic circuit having a first current source which supplies an overdrive current and a second current source which supplies an ordinary current smaller than overdrive current (figs. 1-2; col. 3, lines 7-21; col. 5, lines 1- 30; col. 6, lines 31-67).

Siwiak et al discloses in figure 4, an RF power amplifier 120 where a power supply voltage Vs is applied to the drain of FET 122, through an RF choke 123, and a capacitor 126 is disposed between the drain of the FET 122 and an impedance transformation network 129 (figs. 4-6; col. 3, line 1- col. 4, line 55; col. 5, lines 8-65). It is considered that the capacitors 126 and 206 in figures 4 and 6 are coupled across the power input and the power return. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Siwiak to the modified system of Miyazaki and Hilbert in order to minimize power consumption.

Regarding claims 23-26, Hilbert discloses a circuit (fig. 8), comprising: a differential circuit; and a current source (807, 808, 813 of fig. 8) having an output coupled to the differential circuit; and the current source comprises a transistor (801- 804 of fig. 8) having a drain coupled to the differential circuit, a gate and a source, the capacitor being coupled between the gate and the source (col. 11, line 21- col. 12, line 62; col. 13, line 39- col. 14, line 60).

However, Hilbert does not specifically disclose a current source having an output coupled to the differential circuit, an input, and a capacitor shunting the input.

On the other hand, Miyazaki, from the same field of endeavor, discloses a logic circuit having a first current source which supplies an overdrive current and a second current source which supplies an ordinary current smaller than overdrive current (figs. 1-2; col. 3, lines 7-21; col. 5, lines 1- 30; col. 6, lines 31-67).

Siwiak et al discloses in figure 4, an RF power amplifier 120 where a power supply voltage Vs is applied to the drain of FET 122, through an RF choke 123, and a capacitor 126 is disposed between the drain of the FET 122 and an impedance transformation network 129 (figs.

4-6; col. 3, line 1- col. 4, line 55; col. 5, lines 8-65). It is considered that the capacitors 126 and 206 in figures 4 and 6 are coupled across the power input and the power return. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Siwiak to the modified system of Miyazaki and Hilbert in order to minimize power consumption.

Response to Arguments

2. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marceau Milord whose telephone number is 703-306-3023. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian C. Chin can be reached on 703-308-6739. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-305-9508 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

MARCEAU MILORD

Marceau Milord
Examiner
Art Unit 2682

June 29, 2003